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(54) Method of making integrated circuits

(57) To reduce lateral field oxide protrusions during formation of isolating oxide layers 19 in the vicinity of active regions 13 of integrated circuit devices, the rate of oxidation of areas 18 of silicon semiconductor material adjacent the active regions is enhanced by implantation therein of ions of tin, phosphorus or antimony. The ion dosage should be greater than 5×10^{14} ions/cm² in order to achieve an appreciable effect.

implant enhanced oxd'n

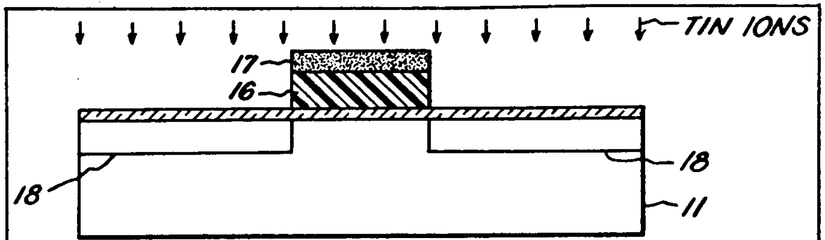

FIG. 3C.

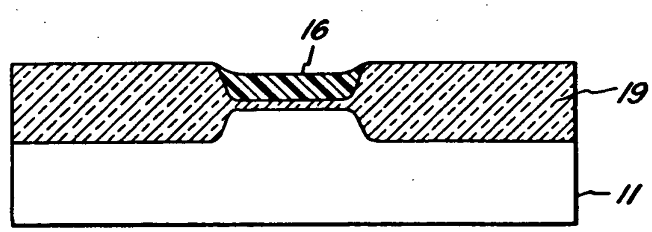

FIG. 3D.

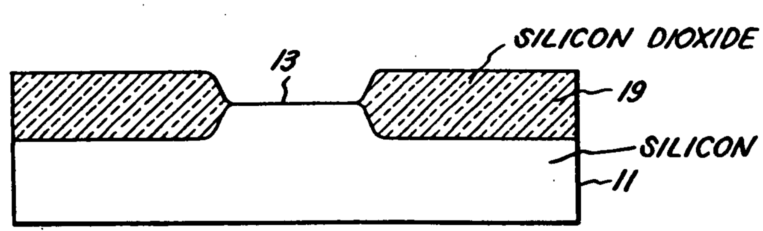

FIG. 3E.

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FIG. 1.

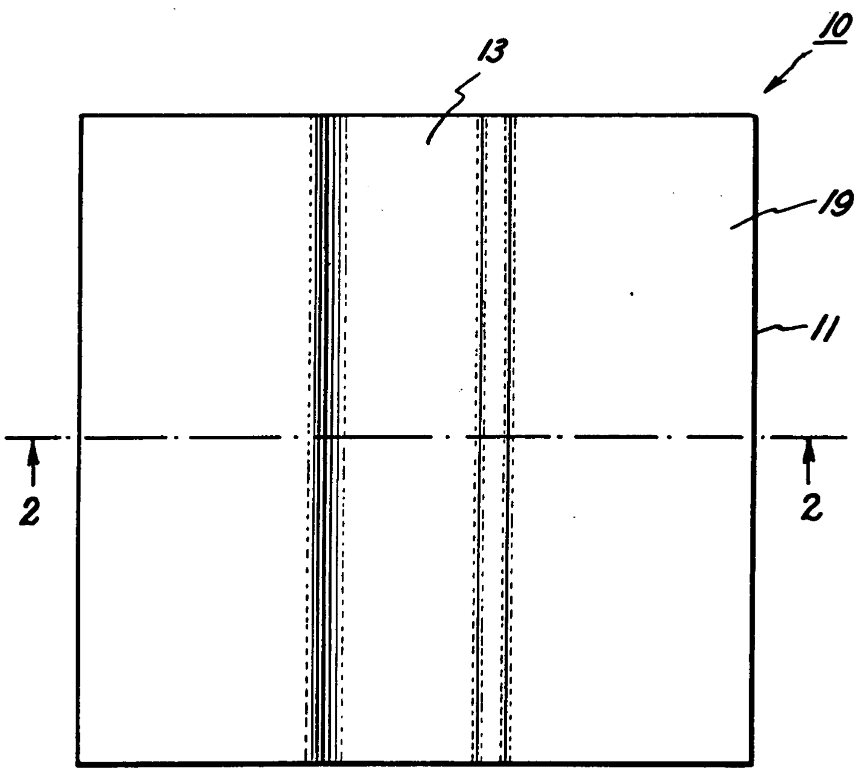


FIG. 2.

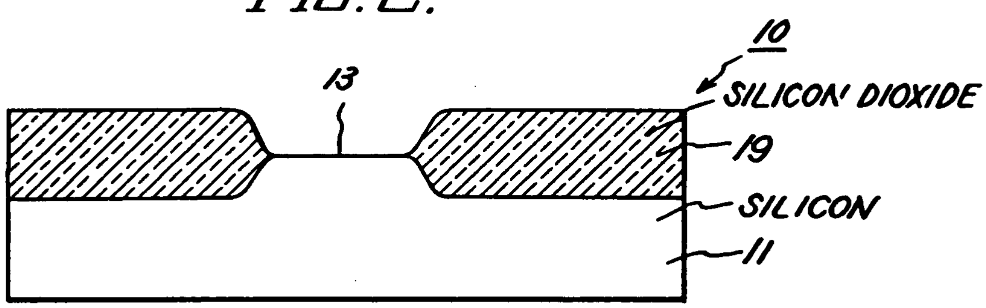


FIG. 3A.

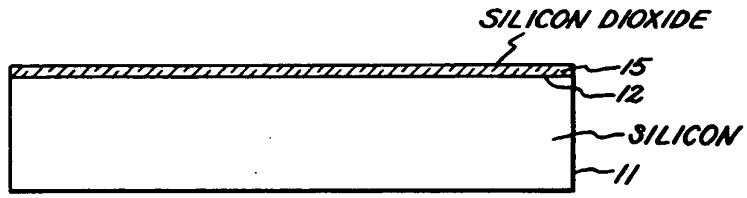


FIG. 3B.

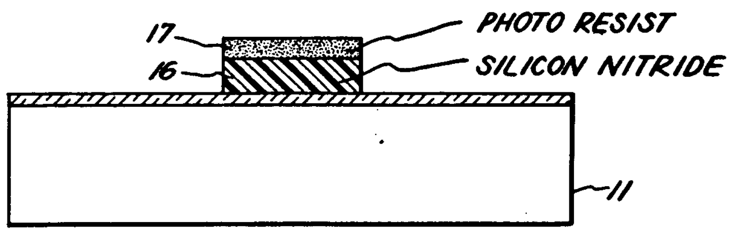


FIG. 3C.

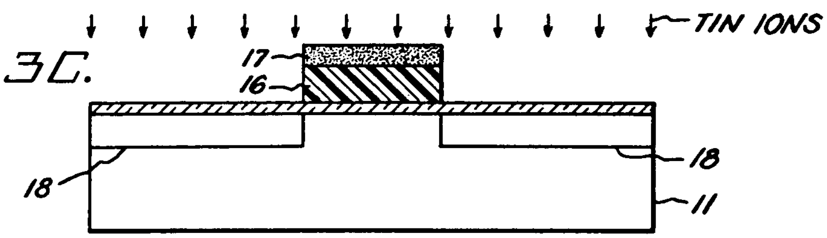


FIG. 3D.

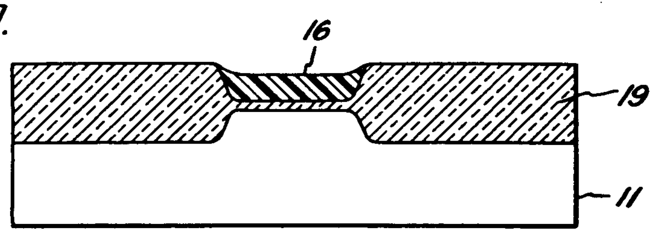
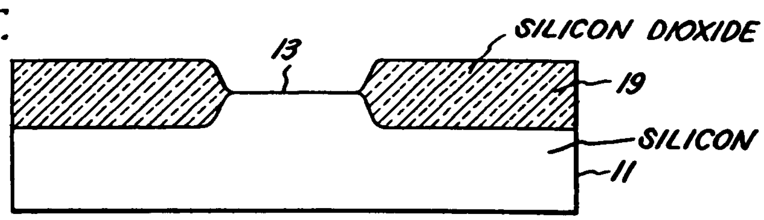


FIG. 3E.



SPECIFICATION

Method of making integrated circuits

The present invention relates in general to a method of making integrated circuits and more particularly for providing on a silicon substrate a thick layer of silicon dioxide contiguous to a surface adjacent region of the substrate.

Integrated circuits comprise a plurality of active components dielectrically isolated on a common silicon substrate. In the making of such circuits the active regions of the substrate on which the active components are formed are masked by a thin layer of silicon dioxide on which is formed a thick layer of silicon nitride. The layer of silicon nitride serves as a mask for etching exposed portions of the layer of silicon dioxide and also for etching recesses in the silicon substrate and for the subsequent oxidation of the silicon in the recesses to form a field oxide which provides the dielectric isolation. The thin layer of silicon dioxide covering the active region of the substrate is provided to buffer the mismatch in thermal expansion between the silicon substrate and the silicon nitride masking layer during processing.

In the oxidation step passage of oxygen laterally through the thin layer of oxide causes growth of oxide in the outer portions of the surface of each of the active regions and produces lateral protrusions of oxide referred to as the "bird's beak" formations. The "bird's beak" formations causes the edges of the field oxide to be shifted, altering the regions predesignated or assigned as the active regions and also produces curvature in the outer portions of the active regions thereby reducing the usable portions thereof.

In carrying out the method of the present invention in accordance with one embodiment thereof, a substrate of silicon semiconductor material having a major surface is provided. A thin layer of silicon dioxide is formed on the major surface of the substrate. A thick layer of silicon nitride is formed over the layer of silicon dioxide. The layer of silicon nitride is patterned to produce a retained portion overlying and in registry with a surface adjacent region of the substrate. A dosage of ions selected from the group consisting of tin, phosphorus and antimony is applied to the substrate through the portion of the major surface thereof unmasked by the retained portion of the layer of silicon nitride. The ions are provided with sufficient energy to penetrate a first average distance below the major surface into the substrate. The dosage is also made sufficiently large to enhance substantially the oxidation of silicon semiconductor material implanted with the ions over silicon semiconductor material unimplanted with the ions. The substrate is then heated in an oxidizing atmosphere to a temperature and for a time to cause the silicon semiconductor implanted with the ions to be converted to silicon dioxide.

The present invention will be further described, by way of example only, with reference to the accompanying drawings, in which:—

Figure 1 is a plan view of a composite body representing a section of an integrated circuit showing a silicon substrate on which is formed a single active region surrounded by an isolating layer of thick silicon dioxide.

Figure 2 is a cross-sectional view of a section of the substrate of Figure 1 taken along section lines 2—2 thereof.

Figures 3A—3E show cross sections of structures representing successive steps in one method of fabricating the composite structure of Figure 1 in accordance with the present invention.

Referring now to Figures 1 and 2, there is shown a composite body 10 representing a section of an integrated circuit made in accordance with the present invention. The composite body includes a substrate 11 having a major surface in which is provided an active region 13 surrounded by a dielectrically isolating layer 19 of thick silicon dioxide. Active components or devices, such as field effect transistors (not shown), are formed in the active region and are isolated from other such active components formed on the substrate by the thick isolating layer 19 of silicon dioxide, referred to as field oxide.

A method of fabricating the composite structure of Figures 1 and 2 in accordance with the present invention will now be described in connection with Figures 3A—3E. Elements of Figures 3A—3E identical to elements of Figures 1 and 2 are identically designated. A substrate 11 of silicon semiconductor material of 10 ohm-cm resistivity and N-type conductivity having a major surface 12 parallel to a (100) crystallographic plane of the substrate is provided. A thin layer 15 of silicon dioxide about 300 Angstroms thick is formed on the major surface 12 by techniques well known in the art, as shown in Figure 3A. For example, the silicon substrate is exposed in an ambient of oxygen at atmospheric pressure and at a temperature of about 1000°C for a period of 30 minutes. Thereafter, a thick layer of silicon nitride is deposited on the surface of the thin layer of silicon dioxide by techniques well known in the art, for example, by chemical vapor deposition. In this process, vapors of silane and ammonia in the ratio of 1 to 200 by volume in a hydrogen carrier are utilized at a temperature of 1000°C and for a time period of several minutes to form a layer of silicon nitride about 1500 Angstroms thick. The layer of silicon nitride is then patterned utilizing photolithographic masking and plasma etching techniques well known in the art to provide a retained portion 16 which overlies and is in registry with the active region 13 of the substrate. The width of the active region 13 may be as small as about 1 micron. A suitable photoresist, such as an azide resist AZ 1470 available from the Shipley Co. of Newton, Mass., is applied over the layer of silicon nitride. After exposure and developing of the photoresist to provide a retained portion thereof, the exposed portions of the silicon nitride unprotected by the photoresist are plasma etched using carbon tetrafluoride with 4% oxygen to provide the retained portion 16 of the silicon

nitride layer. Thereafter, a first dosage of tin ions is applied to the substrate 11 through the major surface 12. The energy of the ions is set sufficiently high to penetrate the thin layer of silicon dioxide and to penetrate to a first average distance 18 below the major surface into the substrate to which silicon will be oxidized, as will be explained below. To provide penetration through an oxide layer of 300 Angstroms to an average distance of 3000 Angstroms into the substrate an energy of 860 keV would be used for tin ions. The retained portion 16 of the silicon nitride layer and the patterned photoresist layer are sufficiently thick to block penetration of the tin ions with the indicated energy and accordingly the surface of the substrate underlying the retained portion of the silicon nitride does not receive any of the dosage of implanted ions. A suitable ion flux density is applied for a time to provide a dosage sufficient to substantially enhance the oxidation rate of the silicon semiconductor material implanted with the impurity. A suitable dosage would be about 5×10^{14} ions per $cm.^2$ and greater. For dosages less than about 5×10^{14} ions per cm^2, it was found that the oxidation rate was not appreciably affected by the implantation. See "Enhanced Oxidation of Silicon by Ion Implantation and Its Novel Applications" by K. Nomura and Y. Hirose in Proceedings of the Fourth International Conference on Ion Implantation in Semiconductors and other Materials held at Osaka, Japan, August 1974, pages 681—688, and published by Plenum Press — New York. The substrate is then heated in an oxidizing atmosphere to a temperature and for a time to cause the silicon semiconductor material surrounding the active region and implanted with tin ions to be oxidized into a thick layer 19 of silicon dioxide. As the tin implantation enhances the rate at which the silicon implanted therewith oxides, oxidation in the vertical direction takes place at a substantially greater rate than the oxidation occurring in the lateral direction. Consequently, lateral oxidation is substantially reduced. Figure 3D shows the resultant structure with substantial reduction in lateral oxidation. For tin ions implanted to an average distance of 3000 Angstroms, the enhanced oxidation rate would occur to about this depth, resulting in a layer of silicon dioxide about 6000 Angstroms thick. Silicon dioxide of such thickness would be obtained by exposing the substrate to steam at atmospheric pressure and a temperature of 1000°C for about 15 minutes. When the layer of silicon dioxide becomes thick, transport to the silicon surface through the layer of thick oxide may become the dominant factor in the oxidation process. To minimize the effect of oxide thickness and to maintain oxidation occurring at the silicon dioxide silicon interface as the dominant process, the oxygen may be supplied at high pressure.

Thereafter, the retained portion of the silicon nitride layer and the underlying retained portion of the layer of silicon dioxide are removed utilizing a suitable etch such as buffered hydrofluoric acid, as shown in Figure 3E. At this point in the process, devices or components such as field effect transistors may be readily formed in the active regions of the substrate so produced.

While in the examples described above, a layer of silicon oxide 300 Angstroms thick and a layer of silicon nitride 1500 Angstroms thick was used, other thicknesses, of course, could be used. The thickness of the silicon dioxide could be in the range from about 200 to about 700 Angstroms and the thickness of the silicon nitride could be in the range from about 1000 to about 2000 Angstroms.

In the process described above, if it is desired to implant ions in the substrate underlying the thick field oxide to increase field thresholds, such implantation could be accomplish subsequent to the implantation of the tin ions but preceding the heating of the substrate to form the thick layer of silicon dioxide. The implantation would be to an average distance greater than the average distance of the tin implantation or to the distance to which oxidation of the silicon will be carried out. If the substrate is N-type conductivity, the field implant could be phosphorus or antimony. If the substrate is P-type conductivity the field implant could be boron. A suitable implant level to increase field thresholds would be about 2×10^{12} ions per cm^2.

While tin is a particularly suitable implant species because it is neutral with regard to imparting a conductivity type to silicon, other species such as phosphorus or antimony may be used with N-type conductivity substrates. When such species are implanted in N-type conductivity substrates with the indicated dosages, i.e., above about 5×10^{14} ions per cm^2, it may not be necessary to use a field implant, as during the oxidation of the silicon implanted with ions of these species, the ions tend to concentrate in the unoxidized silicon.

To provide a structure in which the outer surface of the thick layer 19 of oxide and the active regions lie more nearly in a common plane, the silicon substrate unprotected by the patterned layer 16 of silicon nitride could be etched to the desired depth prior to the oxidation enhancing implantation of ions.

CLAIMS

1. The method of providing in a substrate of silicon semiconductor material having a major surface, a thick layer of silicon dioxide contiguous to a region of said substrate adjacent said major surface which method comprises:

providing said substrate of silicon semiconductor material having a major surface,

forming a thin layer of silicon dioxide on said major surface,

forming a thick layer of silicon nitride on said layer of silicon dioxide,

patterning said layer of silicon nitride to produce a retained portion overlying and in registry with said region of said substrate,

applying a dosage of ions selected from tin,

phosphorous and antimony to said substrate through the portion of said major surface unmasked by said retained portion of said major surface unmasked by said retained portion of said layer of silicon nitride, the energy of said ions being sufficient to penetrate a first average distance below said major surface into the substrate, said dosage being sufficiently large to enhance substantially the oxidation rate of silicon semiconductor material implanted with said ions,

heating said substrate in an oxidizing atmosphere to a temperature and for a time to cause silicon semiconductor material implanted with said ions to be converted to silicon dioxide.

2. A method as claimed in claim 1 wherein the dosage is greater than 5×10^{14} ions cm^{-2}.

3. A method as claimed in claim 1 or claim 2, wherein the thin layer of silicon dioxide is patterned to produce a retained portion overlying and in registry with said region of said substrate.

4. A method as claimed in any one of the preceding claims, wherein the silicon semiconductor material is converted to silicon dioxide to a depth of said first distance.

5. A method as claimed in any one of the preceding claims, wherein retained portions of said layer of silicon nitride and said layer of silicon dioxide overlying said active region are removed.

6. A method as claimed in any one of the preceding claims, wherein the ions are tin.

7. A method as claimed in any one of claims 1 to 5, wherein the ions are phosphorous.

8. A method as claimed in any one of claims 1 to 5, wherein the ions are antimony.

9. A method as claimed in claim 7 or claim 8, wherein the substrate of silicon semiconductor material is of N-type conductivity.

10. A method as claimed in any one of the preceding claims, wherein the thin layer of silicon dioxide has a thickness in the range from 200 to 700 Angstroms and in which said thick layer of silicon nitride has a thickness in the range from 1000 to 2000 Angstroms.

11. A method of preparing a semiconductor material as claimed in claim 1, substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

12. A semiconductor material when produced by a method as claimed in any one of the preceding claims.

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